REMARKS

This Amendment is in response to the Office Action dated October 6, 2006. In the Office Action, claims 1-2, 5-9, 15, 18 and 21 were rejected under 35 USC §103. By this Amendment, the Abstract and claims 1, 4 and 10 are amended. Claims 3 and 11 are canceled and claims 25 and 26 are added. Currently pending claims 1, 2, 4-10, and 12-26 are believed allowable, with claims 1, 10, 12 and 15-24 being independent claims.

AMENDMENTS TO THE ABSTRACT:

The Office Action appears to indicate that the Abstract is too long. By this Amendment, the Abstract is shortened to less than 150 words, as requested in the Office Action.

CLAIM REJECTIONS UNDER 35 USC §103:

Claims 1, 2, 5-9, 15 and 18 and 21 were rejected under 35 USC §103 as being obvious over U.S. Patent No. 6,453,439 to Hattori et al. ("Hattori") in view of U.S. Patent No. 5,905,741 to Matsukuma et al. ("Matsukuma").

Claims 10, 12-14, 16, 17, 19, 20 and 22-24 were rejected under 35 USC §103 as being obvious over U.S. Patent No. 5,856,890 to Hamai et al. ("Hamai") in view of U.S. Patent No. 5,905,741 to Matsukuma et al. ("Matsukuma").

Claims 3, 4 and 11 were indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 1:

Claim 1 is amended to include all the limitations of claim 3, rewriting claim 1 as an independent form of claim 3. As indicated in the Office Action, the limitations of claim 3 are not found in the cited art. Thus, claim 1 is believed allowable over the cited art.

Claims 2 and 4-9:

Claims 2 and 4-9 are dependent on and further limit claim 1. Since claim 1 is believed allowable, claims 2 and 4-9 are also believed allowable for at least the same reasons as claim 1.

Claim 10:

Claim 10 is amended to include all the limitations of claim 11, rewriting claim 10 as an independent form of claim 11. As indicated in the Office Action, the limitations of claim 11 are not found in the cited art. Thus, claim 10 is believed allowable over the cited art.

Claim 12:

A prima facie case for obviousness can only be made if the combined reference documents teach or suggest all the claim limitations. MPEP 2143.

Claim 12 recites, in part, "a below bounded distance decoding control unit for causing the first error correction unit and the second error correction unit to respectively correct errors having smaller distance than limit error correction capabilities of the binary error correction code and the symbol error correction code." Claim 12 further recites, "a bounded distance decoding control unit for causing, if determination is made that the errors are not corrected by the below bounded distance decoding control unit, each of the first error correction unit and the second error correction unit to correct errors by using the limit error correction capability of each of the binary error correction code and the symbol error correction code."

The Office Action has not explained, nor is it apparent, where in either Hamai or Matsukuma is there a teaching or suggestion of a below bounded distance decoding control unit and a bounded distance decoding control unit according to claim 12.

Since all the limitation of claim 12 are not believed to be disclosed in the cited references, the Applicants respectfully submit that claim 12 is allowable.

Claims 13 and 14:

Claims 13 and 14 are dependent on and further limit claim 12. Since claim 12 is believed allowable, claims 13 and 14 are also believed allowable for at least the same reasons as claim 12.

Claim 15:

Claim 15 recites, in part, "wherein the number of bit errors to be corrected per total number of bits of the first data block to which the binary error correction code parity is added is larger than the number of bit errors to be corrected per total number of bits of the second data block to

which the symbol error correction code parity is added." The Office Action states that Hattori does not specifically disclose the above limitations of claim 15, but contends that such a teaching can be found in Matsukuma. Specifically, the Office Action argues this teaching can be found at column 5, line 50 through column 6, line 6 of Matsukuma. The Applicants respectfully disagree with such an interpretation of Matsukuma.

Matsukuma discloses an error correcting method which receives one frame of a digital signal together with a parity code and performs error corrections in both the horizontal and vertical directions. The cited passage of Matsukuma states:

> Compared to the conventional error correcting method, the apparatus additionally has the block data holding unit 5 and the selector 60 If error correction is not normally performed in the first error correction processing, data before error correction is output as error-corrected data from the block data holding unit 5. That is, when a signal has an 82-bit parity code for 190-bit data, error correction can be normally performed for errors of up to 11 bits. However, if 12 or more error bits exist, error correction cannot be normally performed, and even normal bits are also corrected. This consequently increases the number of error bits. If the second and third error corrections are performed in this state, no accurate error correction can be performed, and the number of error bits is increased in some instances. In the present invention, if the number of error bits larger than the number corresponding to a parity code exists, these error bits are left uncorrected. Since the second error correction is performed on the basis of comparison in the vertical direction of a frame, it is highly probable that the number of error bits is decreased to 11 or less in a block in which 12 or more error bits exist in the first error correction processing. When in this state error correction is again performed in units of blocks as the third error correction processing, error bits are nearly completely eliminated. Matsukuma, col. 5, ln. 50 - col. 6, ln. 6.

The Applicants respectfully submit that nowhere in the cited passage, nor elsewhere in Matsukuma is there a teaching or suggestion of the number of bit errors to be corrected per total number of bits of the first data block to which the binary error correction code parity is added is larger than the number of bit errors to be corrected per total number of bits of the second data block to which the symbol error correction code parity is added. Moreover, is quite apparent that Matsukuma does not deal with combining symbol error correction code (such as Reed-Solomon error correction code) with binary error correction codes.

Claim 15 further recites, "a second code encoding step for adding a symbol error correction code for correcting an error by a symbol unit of a predetermined length to each of a plurality of second data blocks into which

the input data sequence is divided in a form different from that of the plurality of first data blocks." The Office Action argues that such a teaching can be found at column 10, lines 32-57 of Hattori. The Applicants respectfully disagree with such an interpretation of Hattori.

The cited passage of Hattori states:

> The second-series information symbol compensation unit 32 performs a processing to convert, into a product code, the pseudo product code coming from the C1 code decoding unit 31, by using the second-series information symbols derived from the second-series information symbol extracting unit 39, and delivers the resultant product code into the first interleave unit 33 in the sequence of the C1 codes.
>
> The second-series information symbol compensating unit 32 has, for example, a configuration as shown in FIG. 5. More specifically, referring to FIG. 5, the second-series information symbol compensating unit 32 has an input terminal 50 for receiving the pseudo product code from the C1 code decoding unit 31, a delay unit 51, and a subtracting unit 52. The second-series information symbol compensating unit 32 also has an input terminal 53 for receiving second-series information symbols from the second-series information symbol extracting unit 39, a zero-symbol adding unit 54, and a C1 code encoding unit 55. The output from the subtracting unit 52 is output to the first interleave unit 33 via the output terminal 56.

The Applicants respectfully submit that there is no teach or suggestion in the cited passage, or elsewhere in Hattori, of a second code encoding step for adding a symbol error correction code for correcting an error by a symbol unit of a predetermined length to each of a plurality of second data blocks into which the input data sequence is divided in a form different from that of the plurality of first data blocks.

For at least these reasons, claim 15 is believed allowable over the cited references. Such allowance is earnestly requested by the Applicants.

Claim 16:

Claim 16 recites, in part, "wherein the number of bit errors to be corrected by the binary error correction code per total number of bits of the first data block is larger than the number of bit errors to be corrected by the symbol error correction code per total number of bits of the second data block." The Office Action states that Hamai does not specifically disclose the above limitations of claim 16, but contends that such a teaching can be found in Matsukuma. Specifically, the Office Action argues this teaching can be found at column 5, line 50 through column 6, line 6 of Matsukuma. The Applicants respectfully disagree with such an interpretation of Matsukuma.

Matsukuma discloses an error correcting method which receives one frame of a digital signal together with a parity code and performs error corrections in both the horizontal and vertical directions. The cited passage of Matsukuma states:

> Compared to the conventional error correcting method, the apparatus additionally has the block data holding unit 5 and the selector 60 If error correction is not normally performed in the first error correction processing, data before error correction is output as error-corrected data from the block data holding unit 5. That is, when a signal has an 82-bit parity code for 190-bit data, error correction can be normally performed for errors of up to 11 bits. However, if 12 or more error bits exist, error correction cannot be normally performed, and even normal bits are also corrected. This consequently increases the number of error bits. If the second and third error corrections are performed in this state, no accurate error correction can be performed, and the number of error bits is increased in some instances. In the present invention, if the number of error bits larger than the number corresponding to a parity code exists, these error bits are left uncorrected. Since the second error correction is performed on the basis of comparison in the vertical direction of a frame, it is highly probable that the number of error bits is decreased to 11 or less in a block in which 12 or more error bits exist in the first error correction processing. When in this state error correction is again performed in units of blocks as the third error correction processing, error bits are nearly completely eliminated. Matsukuma, col. 5, ln. 50 - col. 6, ln. 6.

The Applicants respectfully submit that nowhere in the cited passage, nor elsewhere in Matsukuma is there a teaching or suggestion of the number of bit errors to be corrected by the binary error correction code per total number of bits of the first data block is larger than the number of bit errors to be corrected by the symbol error correction code per total number of bits of the second data block. Moreover, is quite apparent that Matsukuma does not deal with combining symbol error correction code (such as Reed-Solomon error correction code) with binary error correction codes.

Claim 16 further recites, "a second error correction step for correcting an error of each of a plurality of second data blocks, into which the encoded data sequence is divided in a form different from that of the plurality of first data blocks, by minimum distance decoding of a symbol error correction code for error correction by a symbol unit of a predetermined length." The Office Action argues that such a teaching can be found at column 6, line 58 to column 7, line 19 of Hamai. The Applicants respectfully disagree with such an interpretation of Hamai.

The cited passage of Hamai states:

> After inter-track error correction coding, the first controller 5 generates the address of the first memory 2 so as to deliver the data block and inter-track parity from the first memory 2 into an outer error correction encoder 4 in every M1+M2 symbols. The outer error correction encoder 4, using the input M1+M2 symbols as information elements, performs outer error correction coding for generating outer parity in the size of M3 (M3 is a natural number) symbols, and sends out the generated outer parity in the size of M3 symbols into the first memory 2. This is repeated N1.times.L times. The outer error correction encoder 4 composes N1.times.L codewords from data of (M1+M2)xN1xL symbols, and generates parities of M3xN1xL symbols, and sends out to the first memory 2.
>
> After outer error correction coding, the first controller 5 generates the address of the first memory 2 so as to deliver the data block, inter-track parity, and outer parity from the first memory 2 into an inner error correction encoder 6 in every N1 symbols. The inner error correction encoder 6, using the input N1 symbols as information elements, performs inner error correction coding for generating inner parity in the size of N2 (N2 is a natural number) symbols, and sends out the generated inner parity in the size of N2 symbols sequentially into a recording circuit 7. This is repeated (M1+M2+M3)xL times. The inner error correction encoder 6 composes (M1+M2+M3)xL codewords from data in the size of (M1+M2+M3)xN1xL symbols, and generates parities of (M1+M2+M3)xN2xL symbols, and sends out to the recorder 7..

The Applicants respectfully submit that there is no teach or suggestion in the cited passage, or elsewhere in Hamai, of a second error correction step for correcting an error of each of a plurality of second data blocks, into which the encoded data sequence is divided in a form different from that of the plurality of first data blocks, by minimum distance decoding of a symbol error correction code for error correction by a symbol unit of a predetermined length.

For at least these reasons, claim 16 is believed allowable over the cited references. Such allowance is earnestly requested by the Applicants.

Claim 17:

A prima facie case for obviousness can only be made if the combined reference documents teach or suggest all the claim limitations. MPEP 2143.

Claim 17 recites, in part, "a determination step for determining whether the errors of the encoded data sequence are corrected or not in the first below bounded distance decoding step and the second below bounded distance decoding step." Claim 17 further recites, "a bounded distance decoding step for executing, if determination is made that the errors of the encoded data sequence are not corrected, error correction of minimum distance decoding by a limit error correction capability of each of the binary error correction code and the symbol error correction code."

The Office Action has not explained, nor is it apparent, where in either Hamai or Matsukuma is there a teaching or suggestion of a below bounded distance decoding control unit and a bounded distance decoding control unit according to claim 12.

Since all the limitation of claim 12 are not believed to be disclosed in the cited references, the Applicants respectfully submit that claim 12 is allowable.

Claimss 18 and 21:

Claims 18 and 21recite similar limitations as claim 15. As discussed above for claim 15, the Applicants believe that the limitations found in claims 18 and 21 are not disclosed or suggested by Hamai and Matsukuma. For at least these reasons, claims 18 and 21 are believed allowable.

Claims 19, 22 and 24:

Claims 19, 22 and 24 recite similar limitations as claim 16. As discussed above for claim 16, the Applicants believe that the limitations found in claims 19, 22 and 24 are not disclosed or suggested by Hamai and Matsukuma. For at least these reasons, claims 19, 22 and 24 are believed allowable.

Claims 20 and 23:

Claims 20 and 23 recite similar limitations as claim 12. As discussed above for claim 12, the Applicants believe that the limitations found in claims 20 and 23 are not disclosed or suggested by Hamai and Matsukuma. For at least these reasons, claims 20 and 23 are believed allowable.

NEW CLAIMS:

Newly added claims 25 and 26 are believed allowable for at least the same reasons as claims 15 and 16 respectively. No new matter is believed to be introduced by these claims. Support for the subject matter recited in claims 25 and 26 can be found at least at page 13, lines 18-30 of the Application.

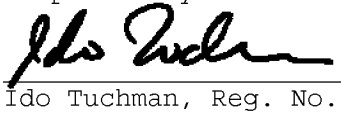
CONCLUSION

In view of the forgoing remarks, it is respectfully submitted that this case is now in condition for allowance and such action is respectfully requested. If any points remain at issue that the Examiner feels could best

be resolved by a telephone interview, the Examiner is urged to contact the attorney below.

No fee is believed due with this Amendment, however, should a fee be required please charge Deposit Account 50-0510. Should any extensions of time be required, please consider this a petition thereof and charge Deposit Account 50-0510 the required fee.

Respectfully submitted,



Dated: January 8, 2007

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MARKUP SHEET

Abstract:

~~Provided is a~~ A communication device which executes proper communications by correcting communication errors caused by noise generated on a transmission line or the like. An encoding device for adding error correction code to an input data sequence is provided with a first code encoding unit for ~~a~~ adding binary error correction code to ~~each of a plurality of~~ first data blocks into which the input data sequence is divided, and a second code encoding unit for adding a symbol error correction code for correcting errors by a symbol unit of a predetermined length to ~~each of a plurality of~~ second data blocks into which the input data sequence is divided in a form different from that of the plurality of first data blocks~~, and characterized in that the number of bit errors to be corrected by the binary error correction code per total number of bits of the first data block to which the binary error correction codes is added is larger than the number of bit errors to be corrected by the symbol error correction code per total number of bits of the second data block to which the symbol error code is added~~.